APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/854,040	05/11/2001	Dale E. Gulick	2000.039400/TT3767	8174

23720	7590	01/25/2005

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EXAMINER
NORRIS, TREMAYNE M

ART UNIT	PAPER NUMBER
2137	

DATE MAILED: 01/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

-- *The MAILING DATE* f *this communication appears on the c ver sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2004*.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1,2,4,6-10,13,15-17,21-24,26 and 31-40* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,6-10,13,15-17,21-24,26 and 31-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1,2,4,6-10,13,15-17,21-24,26,31-40

have been considered but are moot in view of the new ground(s) of rejection.

Information Disclosure Statement

The information disclosure statement filed 10/03/2002 fails to comply with 37

CFR 1.98(a)(2), which requires a legible copy of each U.S. and foreign patent; each

publication or that portion which caused it to be listed; and all other information or that

portion which caused it to be listed. It has been placed in the application file, but the

information referred to therein has not been considered. The non-patent literature was

not received by the examiner.

Claim Rejections - 35 USC § 112

1.   The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of
> making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the
> art to which it pertains, or with which it is most nearly connected, to make and use the same and shall
> set forth the best mode contemplated by the inventor of carrying out his invention.

2.   Claims 34 and 39 are rejected under 35 U.S.C. 112, first paragraph, as failing to

comply with the written description requirement. The claim(s) contains subject matter

which was not described in the specification in such a way as to reasonably convey to

one skilled in the relevant art that the inventor(s), at the time the application was filed,

had possession of the claimed invention. It is unclear where the limitations stated in

claims 25 and 26 are taught within the specification.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1,2,4,6-10,13,15-17,21-24,26,31-40 are rejected under 35 U.S.C. 103(a)

as being unpatentable over Wells et al (US pat 6,687,721), hereinafter Wells '721, and

further in view of Wells et al (US pat 6,792,438), hereinafter Wells '438.

Regarding claim 1, Wells '721 teaches a system, comprising:

a memory configured to store data (col.3 lines 14-17); and

a device coupled to the memory, wherein the device includes a random number

generator (col.3 line 66 thru col.4 line 1),

wherein the random number generator includes:

an entropy register configured to receive bits over a plurality of data lines,

wherein each of the plurality of data lines couples an individual entry in the entropy

register with an entry in a corresponding one of a plurality of registers (col.5 line 58 thru

col.6 line 43).

Wells '721 does not teach the plurality of registers are performance registers.

Wells '438 teaches the plurality of registers are performance registers (col.2 lines 32-35;

col.6 line 66 thru col.7 line 16). These registers represent the definition of applicant's

performance registers for being "any register that updates the least significant bit at a

rate asynchronous to the local and/or system clock." It would have been obvious to one

of ordinary skill in the art at the time of the invention to combine Wells '721's random

number generator with Wells '438's secure hardware random number generator in order

to strengthen and secure the confidentiality of electronic communications for computer

security applications (Wells '438 col.1 lines 18-22).

Regarding claim 2, Wells '721 and Wells '438 in combination teach the system of

claim 1, in addition Wells '721 teaches the random number generator further includes:

an entropy control unit configured to provide a value from the entropy register in

response to a request for a random number (col.6 lines 1-6).

Regarding claim 4, Wells '721 and Wells '438 in combination teach the system of

claim 1, in addition Wells '438 teaches the corresponding entry in the one of the plurality

of performance registers corresponds to the least significant bit entry in each of the

plurality of performance registers (col.6 line 66 thru col.7 line 16).

Regarding claim 6, Wells '721 and Wells '438 in combination teach the system of claim 1, in addition Wells '721 teaches the device includes a processor (col.2 lines 51-59).

Regarding claim 7, Wells '721 and Wells '438 in combination teach the system of claim 1, in addition Wells '721 teaches a bridge coupled between the memory and the device (fig.1).

Regarding claim 8, Wells '721 and Wells '438 in combination teach the system of claim 1, in addition Wells '721 teaches the device is configured to cause data to be stored in the memory (fig.1; col.3 lines 14-17).

Device claims 9,10,13,15 are substantially equivalent to system claims 1, 2,4,6 respectively, therefore claims 9,10,13,15 are rejected for the same reasons.

Random number generator claims 16,17,21 are substantially equivalent to system claims 1,2,4 respectively, therefore claims 16,17,21 are rejected for the same reasons.

Regarding claim 22, Wells '721 teaches a method of generating a random number, the method comprising:

providing a first plurality of bit entries in an entropy register (col.5 lines 60-64);

and

transmitting a bit value from each of a plurality of registers to one of the first

plurality of bit entries in the entropy register (col.6 lines 7-43; col.6 lines 60-67; col.8

lines 45-65).

Wells '721 does not teach the plurality of registers are performance registers.

Wells '438 teaches the plurality of registers are performance registers (col.2 lines 32-35;

col.6 line 66 thru col.7 line 16). These registers represent the definition of applicant's

performance registers for being "any register that updates the least significant bit at a

rate asynchronous to the local and/or system clock." It would have been obvious to one

of ordinary skill in the art at the time of the invention to combine Wells '721's random

number generator with Wells '438's secure hardware random number generator in order

to strengthen and secure the confidentiality of electronic communications for computer

security applications (Wells '438 col.1 lines 18-22).

Regarding claim 23, Wells '721 and Wells '438 in combination teach the system

of claim 22, in addition Wells '721 teaches providing the bit values from each of the first

plurality of bit entries in the entropy register (col.6 lines 60-67; col.8 lines 45-65).

Regarding claim 24, Wells '721 and Wells '438 in combination teach the system

of claim 23, in addition Wells '721 teaches receiving a request for a random number

(col.3 line 35 thru col.4 line 1);

wherein providing the bit values from each of the first plurality of bit entries in the

entropy register comprises providing the bit values from each of the first plurality of bit

entries in the entropy register in response to receiving the request for the random

number (fig.6; col.6 lines 60-67; col.8 lines 45-65).

Regarding claim 26, Wells '721 and Wells '438 in combination teach the system

of claim 23, in addition Wells '721 teaches prior to providing the bit values from each of

the first plurality of bit entries in the entropy register,

providing a control signal to the entropy register (col.6 lines 1-6; col.6 lines 28-

32), and

reading the bit values from each of the first plurality of bit entries in the entropy

register (col.7 lines 1-9).

Claims 31-33,35 are substantially equivalent to claims 22-24,26 respectively,

therefore claims 31-33,35 are rejected for the same reasons.

Computer readable program claims 36-38,40 are substantially equivalent to

method claims 22-24,26 respectively, therefore claims 36-38,40 are rejected for the

same reasons.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tremayne M. Norris whose telephone number is (571) 272-3874. The examiner can normally be reached on M-F 7:30AM-5:00PM alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Caldwell can be reached on (571) 272-3868. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tremayne Norris

January 12, 2005

ANDREW CALDWELL
SUPERVISORY PATENT EXAMINER